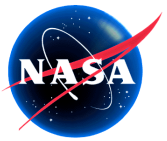

Radiation Mitigation and Power Optimization Design Tools for Reconfigurable Hardware in Orbit

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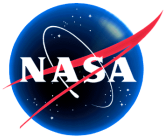
Earth Science Technology Conference

June 30th, 2005



Outline

- Motivation
- CAD Tool Infrastructure
- Radiation Tools and Test Results
- Power Analysis and Optimization Tools
- Conclusions and Future Work

What is an FPGA?

- Mesh of programmable logic blocks with a programmable interconnect
- Define a "Hardware" circuit using "Software" techniques = Firmware
- Two Variants
  - Anti-Fuse – One-time Programmable
  - SRAM-Based – Fully Reprogrammable

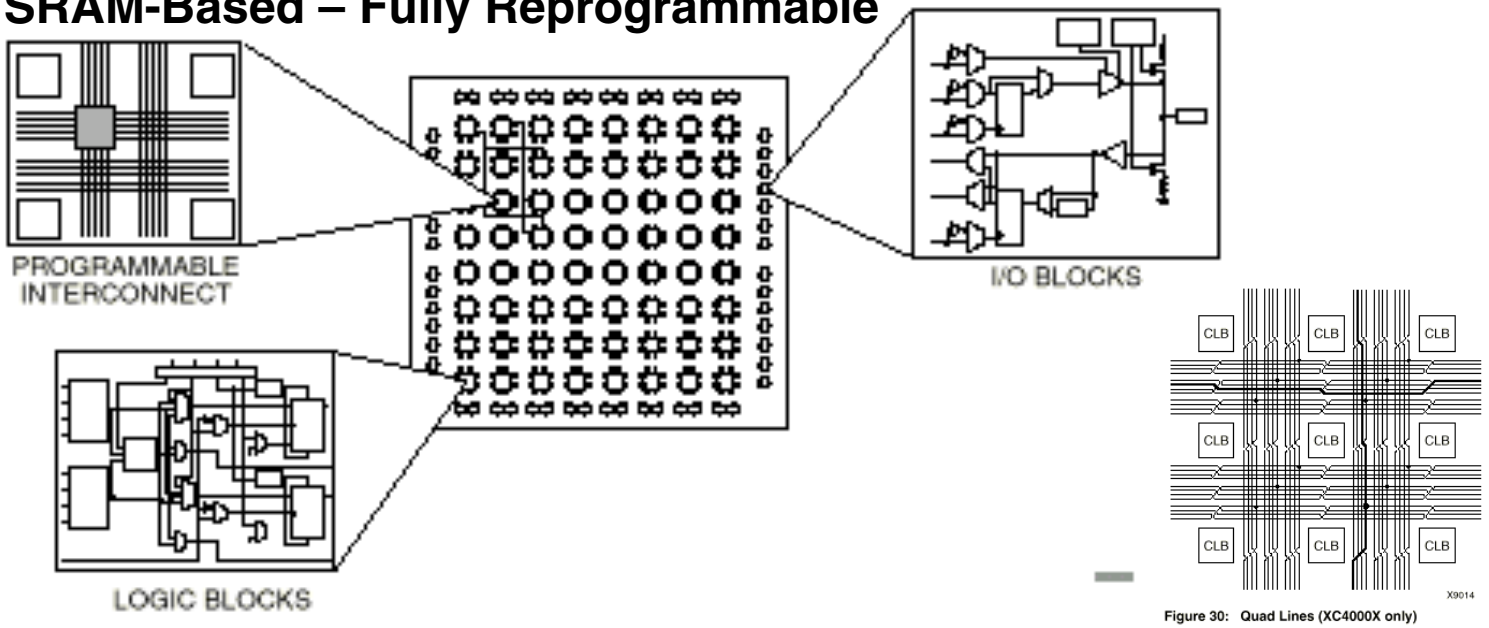
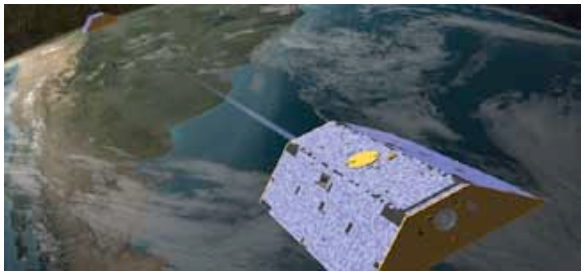


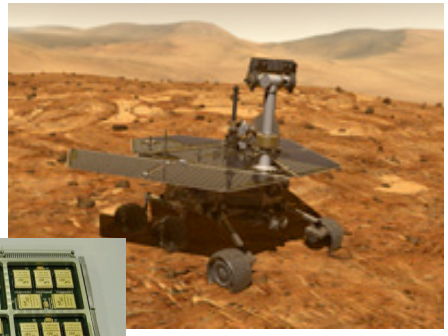
Figure 30: Quad Lines (XC4000X only)

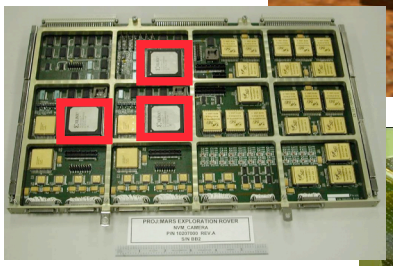
Source: Xilinx XC4000 Data Book

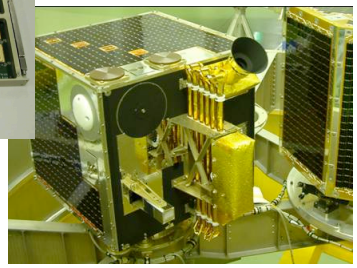
SRAM-Based FPGAs in Space

- **Advantages**
  - 10-100x Processing Performance over Anti-fuse FPGAs
  - Reprogrammable
    - Resource Multiplexing
      - Multi-mission, multi-sensor
    - Mission Obsolescence
      - Update Algorithms
    - Design Flaws
      - Correct in Orbit
- **Gaining Popularity in Space Systems**
  - MARS 2003 Lander (JPL); XQR4062XL
  - MARS 2003 Rover (JPL); XQVR1000
  - GRACE (GSFC); XQR4036XL
  - FedSat (Univ. of Australia); XQR4036XL
  - Optus (Raytheon); XQVR300









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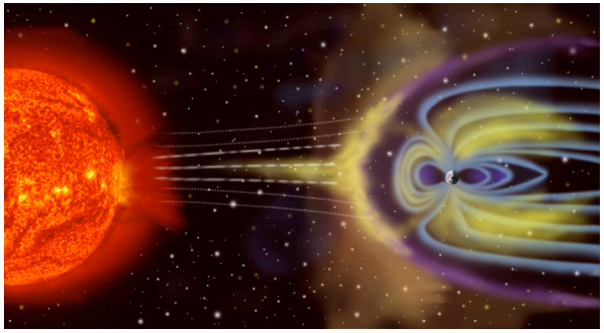
Disadvantages of SRAM-Based FPGAs in Space

- **Radiation Effects**
  - Total Ionizing Dose (TID)
  - Single Event Latchup (SEL)
  - Single Event Upset (SEU)
  - Single Event Functional Interrupt (SEFI)

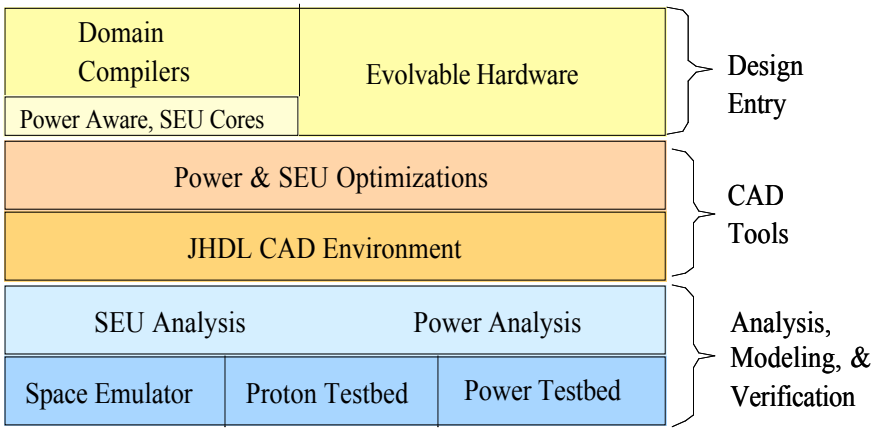


- **Power**
  - Antifuse is more power savvy (20-50% less)
  - Greater Horsepower = Greater Power Consumed
- **SRAM FPGAs vs Anti-fuse FPGAs**
  - Benefits
    - ~10x-100x Performance Gain
    - ~10x Cost Savings
    - ~100-1000x Price Performance Gain
  - Costs
    - Need Software Tools and Techniques for Radiation Mitigation and Power Optimization

Reconfigurable Hardware IN Orbit (RHINO)

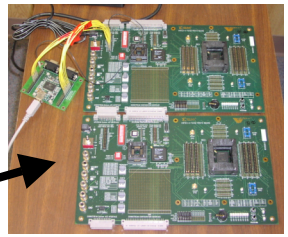
Description and Objectives

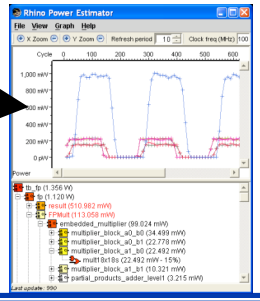
- Facilitate and Automate Designing an SRAM-based FPGA Circuit for the Space Environment
- Create a CAD tool Environment for Xilinx Virtex-II SRAM-based FPGAs capable of
  - **Mitigating Transient Effects**
  - **Minimizing Power Utilization**
  - **Evolving around Hard Faults**
- Provide an Extensible Infrastructure for Future Tests, Techniques, and Architectures



Accomplishments

- Robust EDIF Import Tool
- Half-Latch Removal Tool
- SEU Emulator
- Dynamic Power Visualization
- Detailed Power Analysis Capabilities
- Virtex-II Pre-routed Power Model





Phase	FY03	FY04	FY05
Space Effects and Power Analysis Tools	→		
Space Effects and Power Optimization Tools		→	
Radiation Testing and Validation			→

- **Image Convolution Benchmark**

$TRL_{in} = 3$ ⇒ $TRL_{current} = 4$

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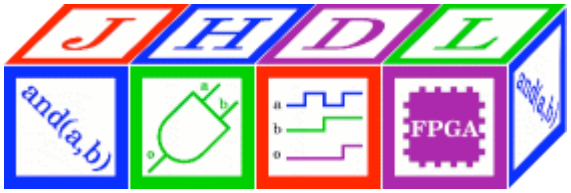
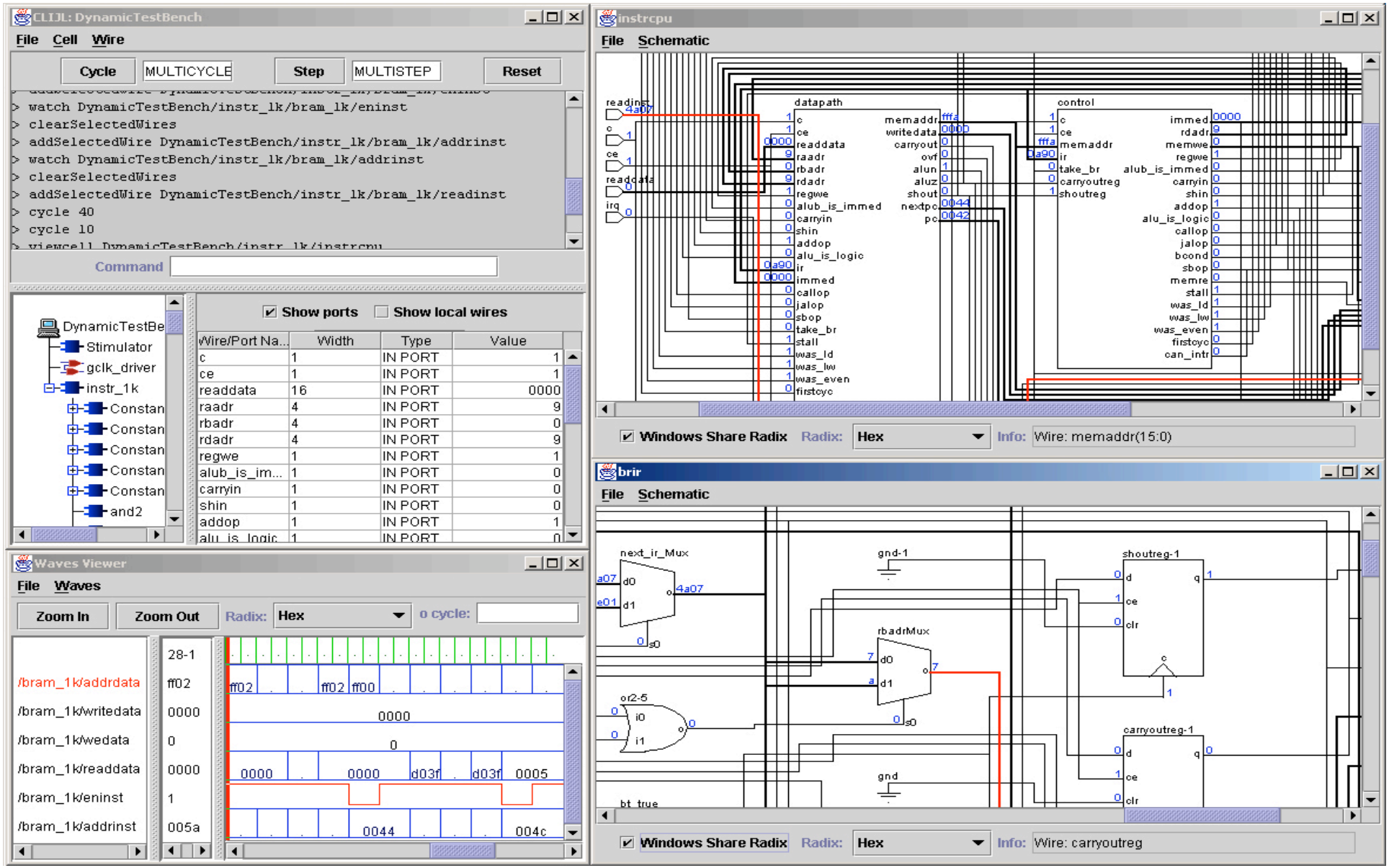
JHDL Overview



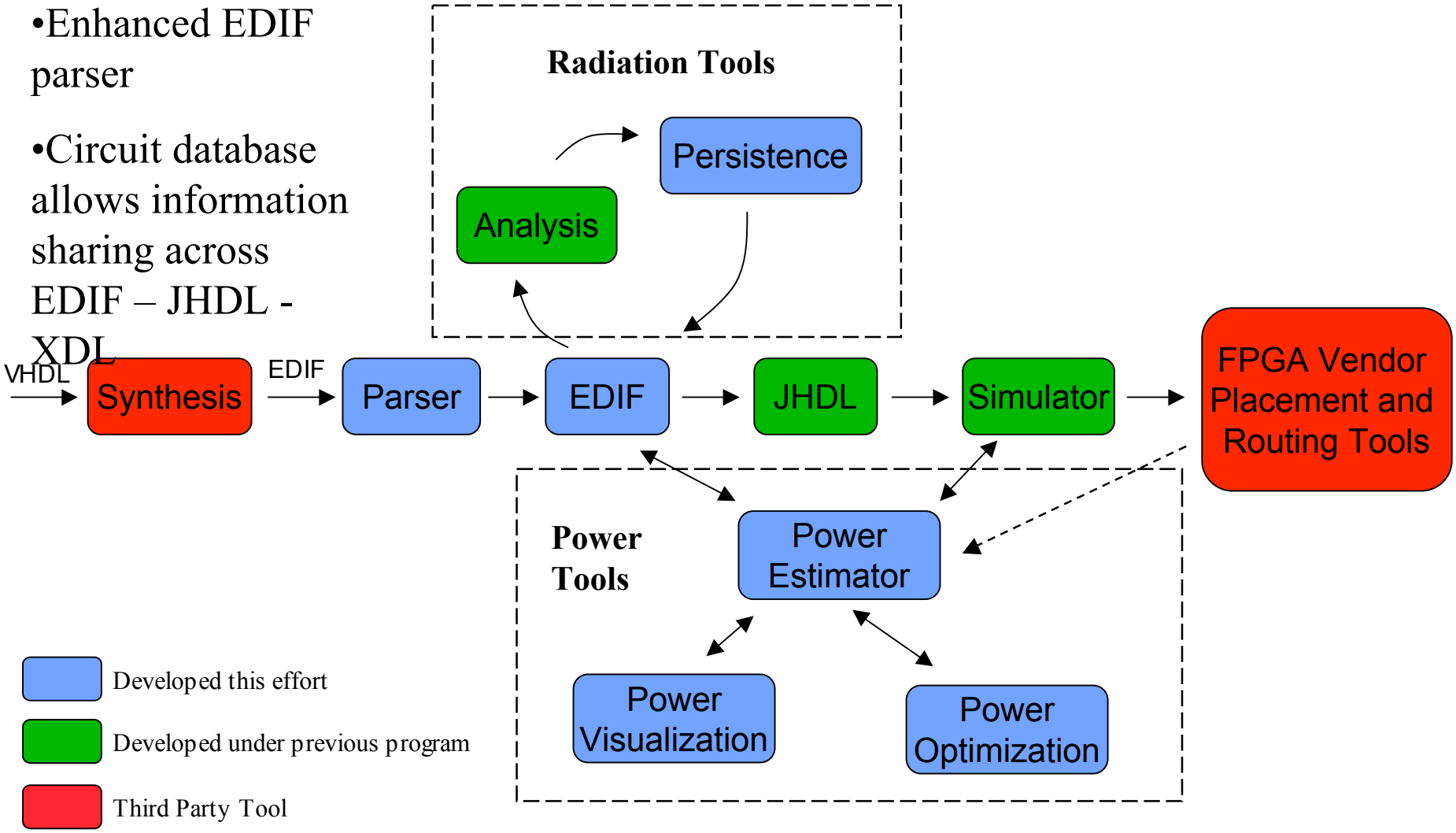
- **Java-based structural design tool for FPGAs**
  - Circuits described by creating Java Classes
    - Instance circuit objects (primitives and modules)
    - Interconnect defined with Wire class objects
  - Design libraries provided for several FPGA families
  - Object Oriented Environment Allows High-level Manipulation of Low-level Circuits
- **JHDL Design Aides**
  - Logic simulator & waveform viewer
  - Circuit schematic & hierarchy browser
  - Module Generators
- **Publicly Available: http://www.jhdl.org**
- **Open Source**
- **Circuit Designer does not need to know Java!**
  - EDIF Import / Export

CAD Tool Unified Environment

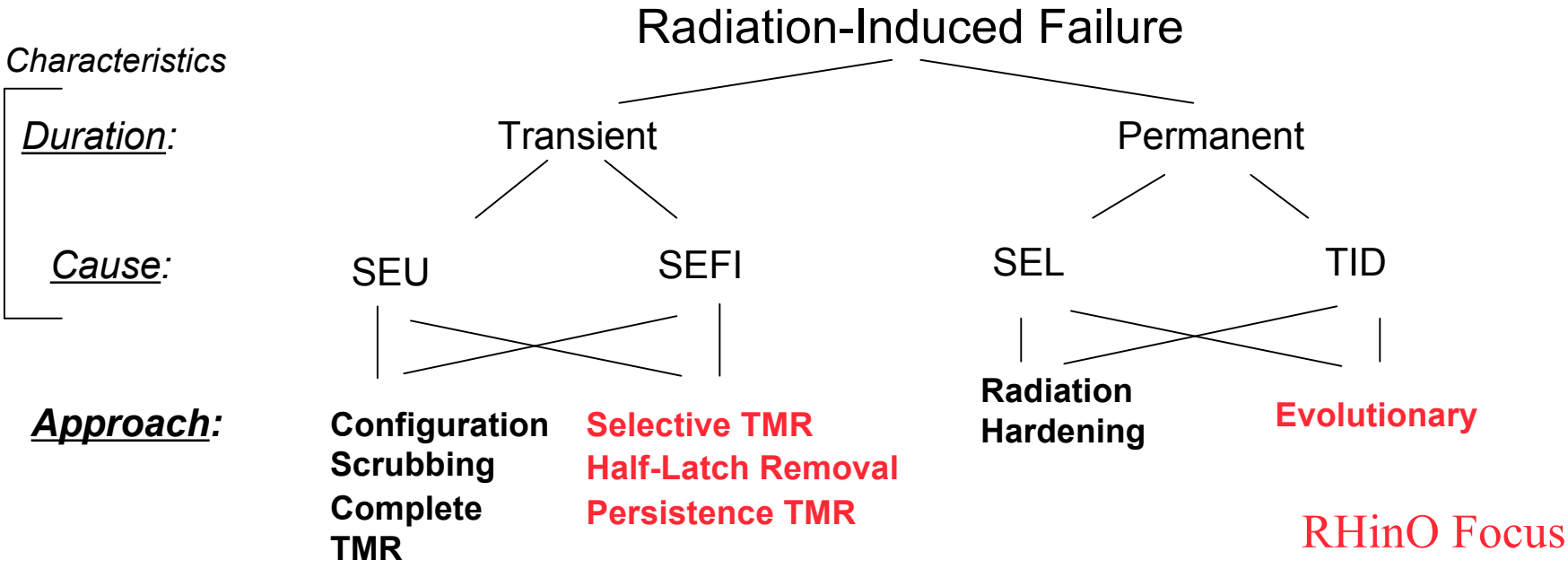


Tool Infrastructure

- Enhanced EDIF parser
- Circuit database allows information sharing across EDIF – JHDL - XDL



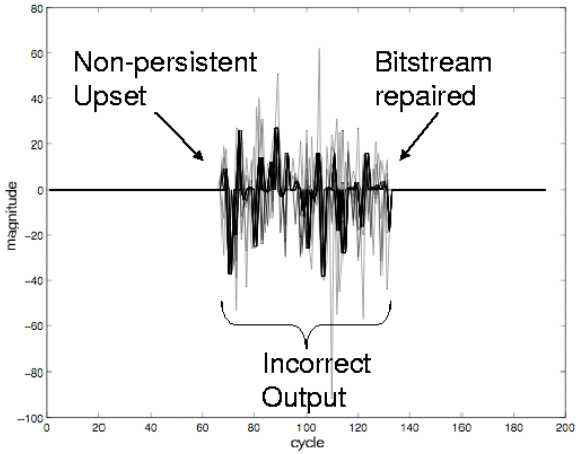
Fault-Handling Techniques for SRAM-based FPGAs

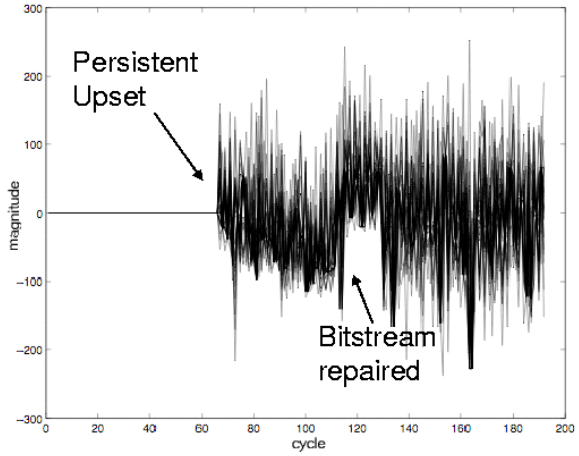


- **Taxonomy of approaches - fit fault-handling level to need**
- **SEU emulator**
  - **Increase effectiveness of laboratory level testing (TRL 4)**
  - **Reduce time / cost of radiation testing**
- **Evolutionary techniques**
  - **Add secondary insurance to radiation hardening**
  - **Potential to move to COTs**

Error Persistence Analysis

- **Some errors persist even after bitstream SEUs are fixed**
- **Evaluate the benefits of selective TMR to cost effectively mitigate this problem (may be much lower cost than full TMR of circuits)**
- **Definitions**
  - ***"Sensitive" bit*: a programming bit that causes one or more errors at the outputs of the FPGA after being upset**
  - ***"Persistent" bit*: a sensitive programming bit that causes an error that persists at the outputs once being upset and then repaired**





Output differences between Golden and Design Under Test

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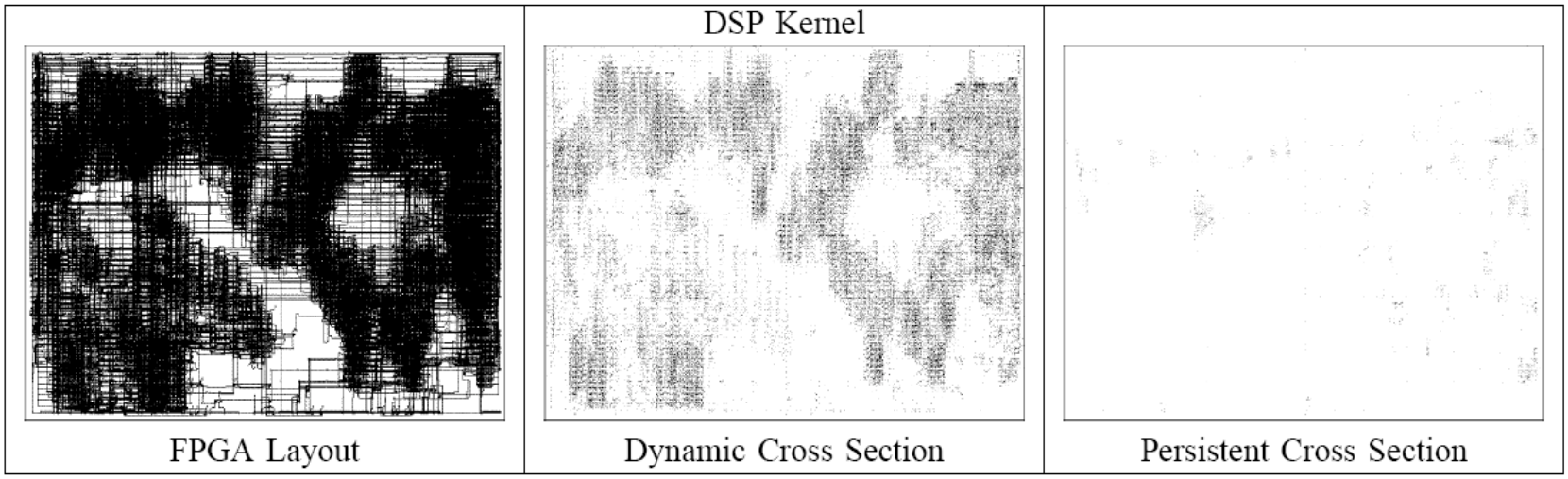
SEU Sensitivity Maps



- **Potential persistence benefit**
  - **Orbit: LEO, 400 km, 51.6 degree inclination**
  - **Conditions: Stormy Solar Maximum**
  - **DSP Application: Snap-shot recorder**
  - **If intolerant of brief data loss**
    - **Mean Time Between Failures (MTBF): 13.6 days**
  - **If tolerant to brief data loss**
    - **MTBF: 215.5 days (persistent failures only)**
    - **Mean Time Between Data Loss (MTBDL): 13.9 days**
- ***If brief data loss can be tolerated, more than a 16x improvement in MTBF for this application***

Error Persistence Mitigation

- **Tools available**
  - **Analysis tool for identifying the flip-flops affecting persistence**
    - **Initial version complete**
    - **Used in accelerator analysis Jan 2005**
  - **TMR/Selective TMR Tool**
    - **Using new graph representation of circuits to ease analysis**
- **Selective TMR tool to be tested with Virtex-II during August accelerator testing (UC-Davis)**
  - **Use "synthetic" designs with known persistence**

Multiple Bit Upset (MBU) Analysis

- **Determining how frequently a single ionized particle causes multiple configuration bits to be upset.**
- **Looking at the trend across multiple families of FPGAs**
  - **Virtex (DOE funded)**
  - **Virtex-II (NASA funded)**
  - **Virtex-II Pro (DOE funded)**
  - **Virtex-4 (DOE funded)**
- **Main Issue: Do MBUs cause TMR (or other mitigation methods) to fail?**
  - **If so, how often?**
  - **Can we mitigate against these problems?**

MBU Methodology

- **Sample configuration upsets for all architectures**
  - **At rate that ensures that significant amount of data while minimizing false MBUs**
- **Perform bit clustering to identify MBUs of maximal size**
- **Identify the function of bits affected (with help from Xilinx)**
- **For identified functions, consider implications on TMR**
  - **Could it affect multiple TMR domains?**
  - **If so, how often might this particular situation occur?**
- **Predict affect of MBUs on TMR based on**
  - **Frequency of MBUs due to protons**
  - **Frequency of MBUs affecting multiple domains of TMR**

MBU Progress: Accelerator (Jan 05)

- **Collected data for Virtex, Virtex-II (2V250 and 2V1000), and Virtex-4 (4VLX25)**
- **Results**
  - **Virtex: MBUs about .045% of total events**
  - **Virtex-II 2V1000: MBUs about 1.07% of total events (very similar to previous 2V250 results)**
  - **Virtex-4: Analysis not finished, real-time feedback suggests about 1% of events may be MBUs**

Virtex-II 1000 Details

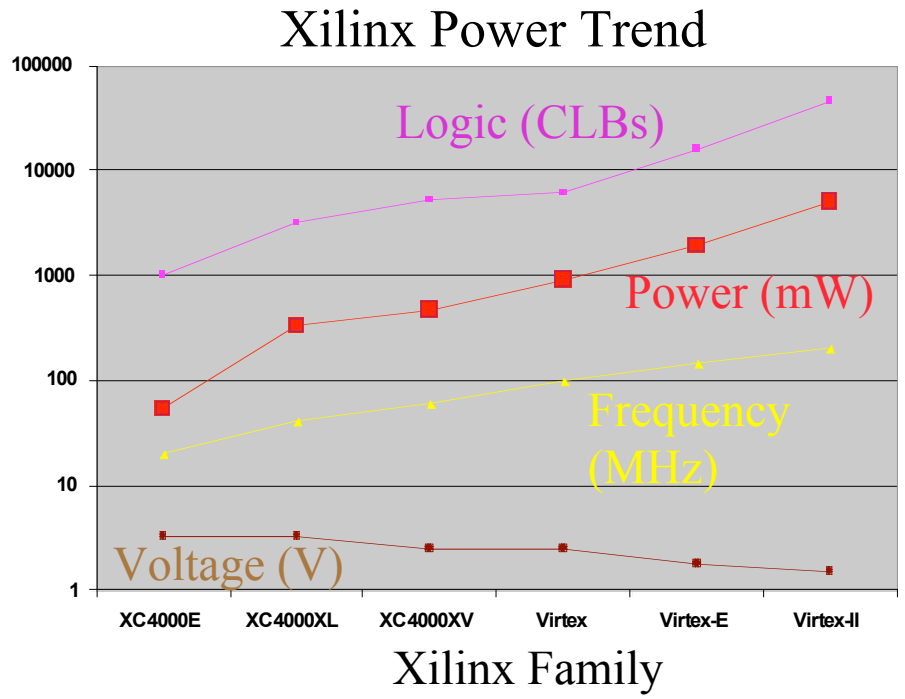
- **Clusters**
  - **1-bit: 199641 (98.92%)**
  - **2-bit: 2164 (1.07%)**
  - **3-bit: 12 (0.006%)**
  - **4-bit: 1 (0.0005%)**
- **Adjacencies**
  - **Within column: 1944 (88.48%)**
  - **Within row: 143 (6.51%)**
  - **Diagonals: 110 (5.01%)**

Not likely to affect TMR, analysis ongoing

- **MBU Bits by resource**
  - **IOB1: 32 (0.73%)**
  - **IOB2: 213 (4.88%)**
  - **BRAM Int.: 1056 (24.18%)**
  - **BRAM: 161 (3.69%)**
  - **CLB: 2906 (66.53%)**
  - **GCLK: 0 (0%)**

RHinO Power Tools

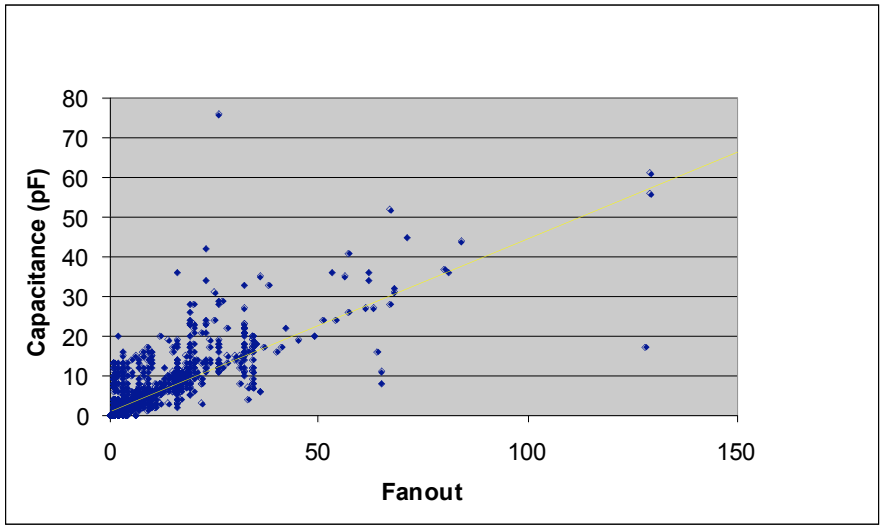
- **Power consumption has become a primary design constraint for some systems, but this is not reflected in modern FPGA tools.**
- **Push power analysis, visualization, and optimization to front of the tools chain:**
  - ***Analyze*** **power consumption at logic simulation with two levels of accuracy**
    - **Pre-place-and-route, using heuristic estimates based on fanout**
    - **Back-annotated with precise post-place-and-route RC data**
  - ***Visualize*** **by providing intuitive views to help the designer rapidly find and correct inefficient circuits, operating modes, data patterns, etc.**
  - ***Optimize*** **systems by automatically identifying problem paths and suggesting improvements**



Pre-placement and Routing Power Estimation

$$Power = \sum (\%toggle)(Freq_{Clock})(Cap_{Component} + Cap_{Wire})$$

- **Toggle rate and frequency available from simulation**
- **Component capacitance**
  - **Import from Xpower**
  - **Literature**
  - **Component information exists at synthesis**
- **Wire capacitance unknown**
  - **Need predictive models**
- **Capacitance vs**
  - **Fanout**
  - **Programmable Interconnect Points**
  - **Wire Length**
  - **Total Number of Nets**
  - **Total Number of Components**
- **Which relationships maintain correlation from synthesis to place and route?**
  - **Optimizer removes components, nets**

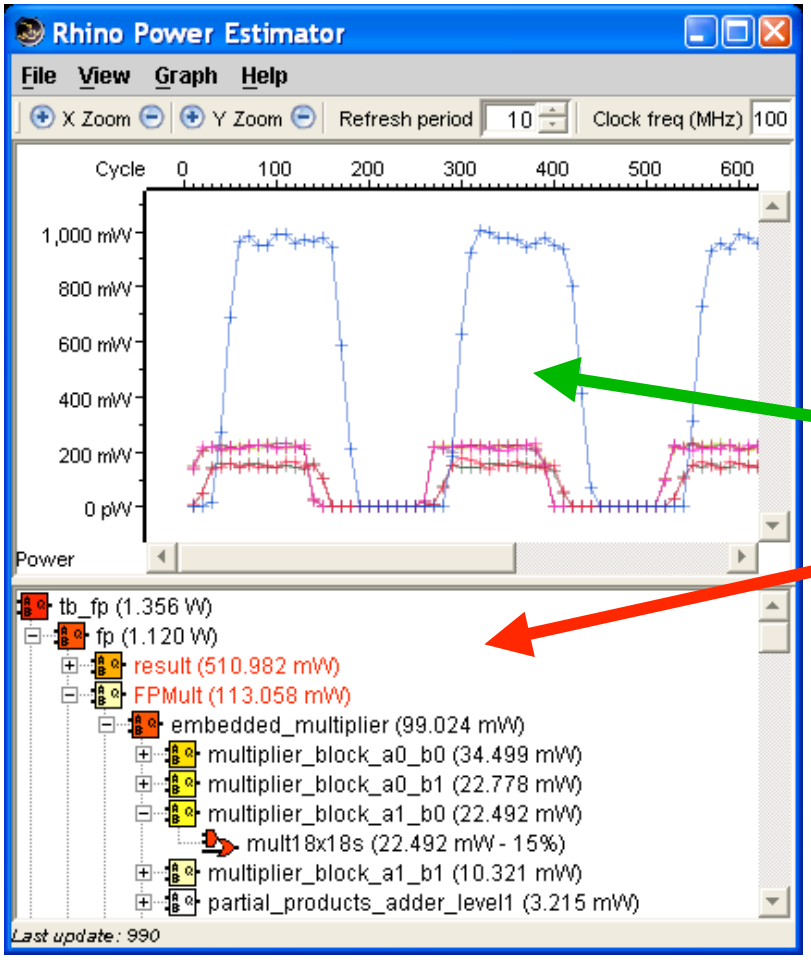


Model Results

Relationship	Comments	Average Error vs Xpower
Unity	Original model	47.4%
Fanout	Relationship generally holds well through design flow	4.3%
Total Number of Nets	Synthesis Tool Dependant	27.8%
Total Number of Components	Synthesis Tool Dependant	23.5%
Total Number of PIPs	Not available at synthesis level	NA
Wire Length	Not available at synthesis level	NA
Source / Destination Type (Mult, BRAM, slice)	Currently Investigating	TBD

- **Further wire-length prediction modeling refinement ongoing**
  - Low fan-out variance, glitching

Power Analysis Tool Status

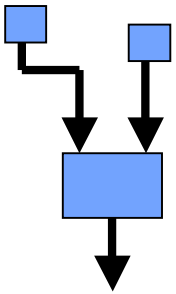


- **Analysis and visualization tool complete**
- **Power estimation based on one of three Power Models**
  - **Generic Toggle Model**
  - **Virtex II Power Model**
  - **Actual Routed Circuit**
- **Two views:**
  - **Instantaneous vs. cumulative power consumption over time**
  - **Sorted tree view of "worst offenders"**
- **Integrated "cross-probing" with existing JHDL tools**
  - **Unified Environment**
  - **Allows Experimentation**
  - **Smart Re-use of CPU Memory**
- **Help rapidly identify inefficient circuits and operating modes**
- **Per-cell / per-bit granularity**

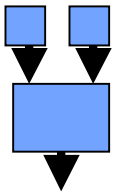
Power Optimization

- **Influence Xilinx Place&Route tools for power efficiency**
  - **Minimize clock/wire lengths of high power nets**
- **Use power analysis tools to identify hot-spots and generate constraints**
  - **Timing constraints on non-clock signals**
  - **Location constraints on sink flip-flops of clock signals**

Timing Constraint Optimization

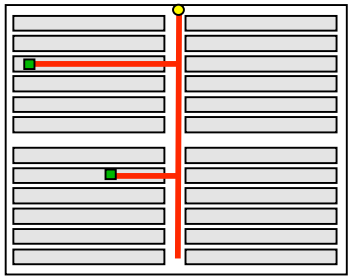


Default Constraints
Constraint Freq : 50 MHz
Operating Freq : 50 MHz
Poor Power Efficiency

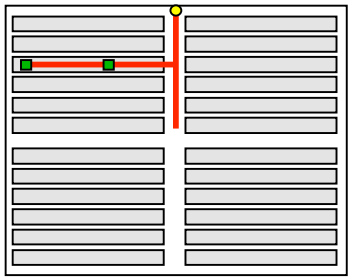


Power Timing Constraints
Constraint Freq : 100 MHz
Operating Freq : 50 MHz
Better Power Efficiency

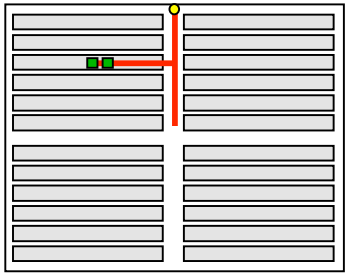
Placement Optimization



Poor

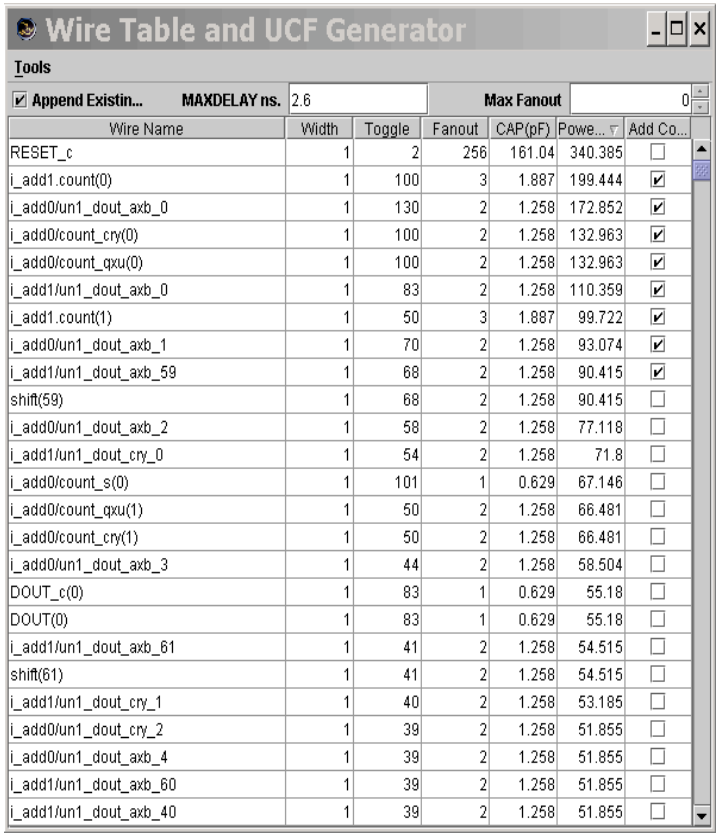


Better



Optimal

Timing Constraint Power Optimization Preliminary results



Wire Name	Width	Toggle	Fanout	CAP(pF)	Powe...	Add Co...
RESET_c	1	2	256	161.04	340.385	☐
i_add1.count(0)	1	100	3	1.887	199.444	☑
i_add0/un1_dout_axb_0	1	130	2	1.258	172.852	☑
i_add0/count_cry(0)	1	100	2	1.258	132.963	☑
i_add0/count_qxu(0)	1	100	2	1.258	132.963	☑
i_add1/un1_dout_axb_0	1	83	2	1.258	110.359	☑
i_add1.count(1)	1	50	3	1.887	99.722	☑
i_add0/un1_dout_axb_1	1	70	2	1.258	93.074	☑
i_add1/un1_dout_axb_59	1	68	2	1.258	90.415	☑
shift(59)	1	68	2	1.258	90.415	☐
i_add0/un1_dout_axb_2	1	58	2	1.258	77.118	☐
i_add1/un1_dout_cry_0	1	54	2	1.258	71.8	☐
i_add0/count_s(0)	1	101	1	0.629	67.146	☐
i_add0/count_qxu(1)	1	50	2	1.258	66.481	☐
i_add0/count_cry(1)	1	50	2	1.258	66.481	☐
i_add0/un1_dout_axb_3	1	44	2	1.258	58.504	☐
DOUT_c(0)	1	83	1	0.629	55.18	☐
DOUT(0)	1	83	1	0.629	55.18	☐
i_add1/un1_dout_axb_61	1	41	2	1.258	54.515	☐
shift(61)	1	41	2	1.258	54.515	☐
i_add1/un1_dout_cry_1	1	40	2	1.258	53.185	☐
i_add0/un1_dout_cry_2	1	39	2	1.258	51.855	☐
i_add0/un1_dout_axb_4	1	39	2	1.258	51.855	☐
i_add1/un1_dout_axb_60	1	39	2	1.258	51.855	☐
i_add1/un1_dout_axb_40	1	39	2	1.258	51.855	☐

- Power is reduced by up to 11.8% on test circuit
- Can vary which nets to constrain and by how much
  - More constraints not necessarily better
- Circuits still meet original timing specification requirements
- Working on optimization algorithms and automating

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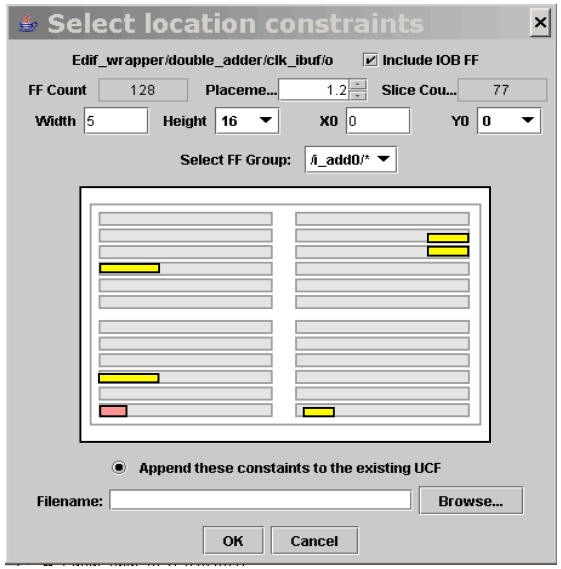
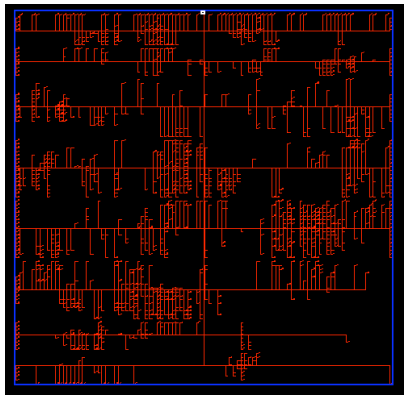
Location Constraint Power Optimization Preliminary Results

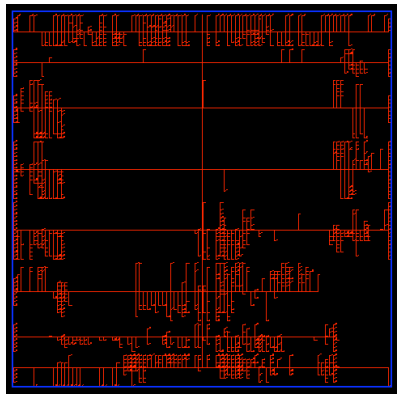
- Individual clock net improvement up to 57%
- Achieve up to 22.9% <u>total</u> power improvement
- Circuits still meet timing requirement
- Also working on optimization algorithms and automation
- Two approaches are not mutually exclusive



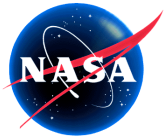
Tool Interface



Unoptimized



Optimized

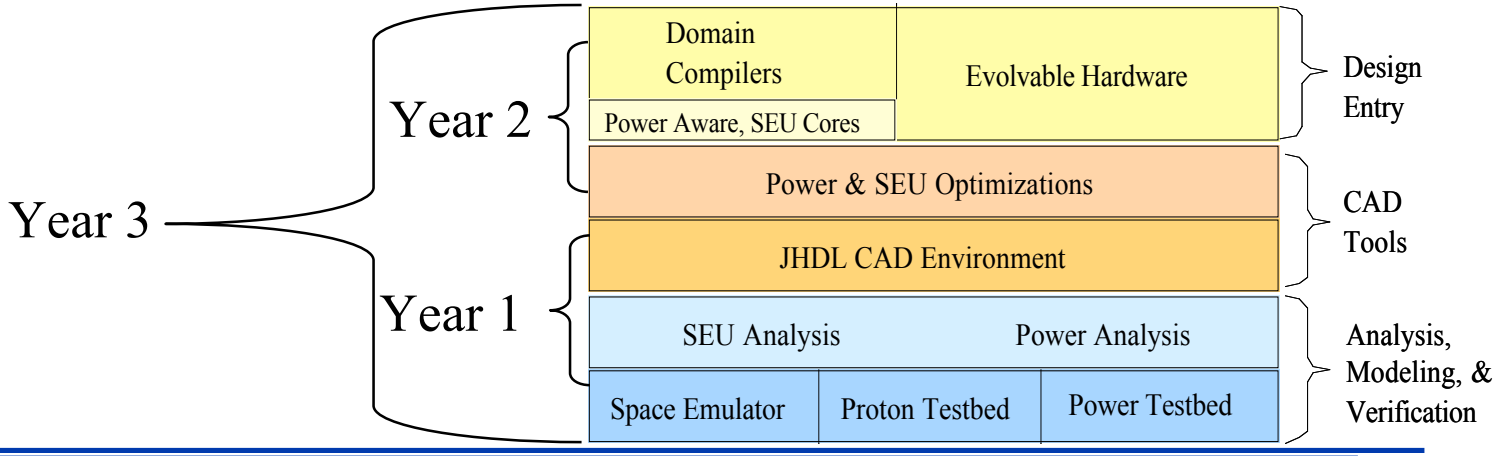


Summary

- **Tool infrastructure**
  - **Supports radiation and power tool modules**
  - **Open source: http://www.jhdl.org**
- **Radiation Tools**
  - **SEU Emulator development completed**
  - **Half-latch removal tool available**
  - **Persistence analysis tool completed**
  - **MBU analysis underway**
  - **Contact LANL for tool licensing**
- **Power Tools**
  - **Power analysis tools completed**
  - **Power optimization tool rev 0 completed**
    - **Adding optimization algorithms in rev 1**
  - **Open source: http://rhino.east.isi.edu**

Future Work

- **Power**
  - Power Optimization Algorithms
  - Waveform Analyzer
- **Radiation**
  - Complete Error Persistence
  - MBU Final Analysis
  - Evolution Techniques
- **Integrate Tool Suite**
  - Continue to clean-up and add functionality
- **Module Generators**
  - Generators with both SEU mitigation and power optimization options
- **Verify Combined Results**
  - Analyze power of radiation mitigation techniques
  - Obtain final results for radiation robustness and power optimization on image convolution benchmark



Background

Further Reading: Team Publications

- "*Reducing Energy in FPGA Multipliers Through Glitch Reduction*", Nathan Rollins and Michael Wirthlin, Brigham Young University, University DSPACE archive, https://dspace.byu.edu/handle/1877/61
- *"SEU Induced Error Propagation in FPGAs"*, Keith S. Morgan, Michael Caffrey, Paul Graham, D. Eric Johnson, Brian H. Pratt, and Michael J. Wirthlin. Accepted for presentation and publication at the IEEE Nuclear NSREC conference, 2005
- *"Persistent Errors in SRAM-based FPGAs"*, D. Eric Johnson, Keith S. Morgan, Michael J .Wirthlin, Michael Caffrey, and Paul Graham, 7th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD), September 2004.
- *"Evaluation of Power Costs in Applying TMR to FPGA Designs"*, Nathan Rollins, Michael J. Wirthlin, Michael J .Wirthlin, Michael Caffrey, and Paul Graham, 7th Annual International Conference on MAPLD, September 2004.
- *"Validation of an FPGA Fault Simulator"*, D. Eric Johnson, Michael Caffrey, Paul Graham, Nathan Rollins, and Michael J .Wirthlin, IEEE Transactions on Nuclear and Space Radiation Effects (NSREC), December 2004.
- "Synthesis Level Power Estimation for FPGAs," French, Wang, Anderson, Wirthlin, IEEE Symposium on Field-Programmable Custom Computing Machines, April 2005.
- "A Power Efficient Image Convolution Engine for Field Programmable Gate Arrays ," French, Matthew, 7th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD), September 2004.